CLAIMS

The invention claimed is:

1. A semiconductor device comprising:

a chip;

a plurality of first blocks on the chip;

a system bus on the chip coupled with the first blocks;

an external bus for coupling a dual one of the first blocks to a plurality of second blocks external to the chip; and

a single on-chip multi-jurisdictional arbiter adapted to receive requests for ownership of the system bus and of the external bus, to rank all the received requests according to a programmable priority schedule, to transmit a first grant signal to the dual first block regarding a first ownership of the external bus, and to transmit a second grant signal regarding a second ownership of the system bus to another one of the first blocks that is concurrent with the first ownership.

2. The device of claim 1, wherein the arbiter includes

a request decoder adapted to receive a request signal from the dual first block operating as a master of the external bus and another request signal from another one of the first blocks operating as a master of the system bus;

a priority scheduler to receive an output of the request decoder;

a system bus master selector to receive an output of the priority scheduler containing data about a first top priority and further adapted to transmit the first grant signal responsive to the first top priority; and

an external bus master selector to receive an output of the priority scheduler containing data about a second top priority and further adapted to transmit the second grant signal responsive to the second top priority.

3. The device of claim 1, further comprising:

a first bus switch on the chip;

an auxiliary system bus on the chip coupled to the system bus through the first bus switch; and

a plurality of third blocks on the chip coupled with the auxiliary system bus,

wherein the arbiter is adapted to transmit a third grant signal to one of the third blocks regarding a third ownership of the auxiliary system bus that is to be concurrent with the first ownership.

4. The device of claim 1, wherein

the system bus is split into a left portion and a right portion separated by a second bus switch, and

the arbiter is adapted to transmit a control signal to the second bus switch.

5. A device comprising:

a semiconductor chip;

a system bus on the chip;

an external bus;

a third path distinct from the system bus and the external bus; and

a plurality of first blocks on the chip coupled directly with the system bus, wherein

at least one of the first blocks is an external memory controller coupled to the external bus and adapted to control at least one memory device that is external to the chip, and

another one of the first blocks is a multi-jurisdictional multi-channel general direct memory access block that is coupled with the external memory controller via the third path.

6. The device of claim 5, wherein the external memory controller includes:

an external bus controller to control the external bus;

an address and control multiplexer adapted to receive address and control inputs from both the system bus and the multi-jurisdictional multi-channel general direct

memory access block, and adapted to transfer one of the received address and control inputs to the external bus controller;

a write data multiplexer adapted to receive data inputs from both the system bus and the multi-jurisdictional multi-channel general direct memory access block, and adapted to transfer one of the received data inputs to the external bus controller; and

a read data demultiplexer adapted to receive data inputs from the external bus controller, and adapted to transfer the received data inputs to one of the system bus and the chip multi-jurisdictional multi-channel general direct memory access block.

7. The device of claim 6, wherein

the address and control multiplexer, the write data multiplexer, and the read data demultiplexer are controlled by inputs from the external bus controller.

8. The device of claim 6, further comprising:

at least one buffer coupled between the external bus controller and the external bus.

9. The device of claim 5, further comprising:

an on-chip multi-jurisdictional arbiter to transmit a first grant signal to one of the first blocks regarding a first ownership of the system bus and to transmit a second grant signal to the external memory device regarding a second ownership of the external bus that is concurrent with the first ownership.

10. The device of claim 9, wherein the arbiter includes

a request decoder to receive a request signal from one of the external memory device and one of the first blocks;

a priority scheduler to receive an output of the request decoder;

a system bus master selector to receive a first output of the priority scheduler containing data about a first top priority and further adapted to transmit the first grant signal responsive to the first top priority; and

an external bus master selector to receive a second output of the priority scheduler containing data about a second top priority and further adapted to transmit the second grant signal responsive to the second top priority.

11. The device of claim 10, wherein the arbiter further includes

a system bus slave selector to transmit a select signal to one of the first blocks responsive to a third output originating from the priority scheduler.

12. The device of claim 11, wherein

the third output is first received and decoded by the system bus master selector, and

the system bus slave selector is adapted to receive from the system bus master selector a corresponding signal responsive to the third output.

13. The device of claim 9, wherein the external memory controller includes:

an external bus controller to control the external bus;

an address and control multiplexer adapted to receive address and control inputs from both the system bus and the multi-jurisdictional multi-channel general direct memory access block according to the first ownership, and adapted to transfer one of the received address and control inputs to the external bus controller according to the second ownership;

a write data multiplexer adapted to receive data inputs from both the system bus and the multi-jurisdictional multi-channel general direct memory access block, and adapted to transfer one of the received data inputs to the external bus controller; and

a read data demultiplexer adapted to receive data inputs from the external bus controller, and adapted to transfer the received data inputs to one of the system bus and the multi-jurisdictional multi-channel general direct memory access block.

14. The device of claim 13, wherein

the address and control multiplexer, the write data multiplexer, and the read data demultiplexer are controlled by inputs from the external bus controller.

15. The device of claim 13, further comprising:

at least one buffer coupled between the external bus controller and the external bus.

16. The device of claim 13, wherein

the external bus controller is adapted to receive an external bus grant signal from the arbiter for controlling the external bus as a master.

17. The device of claim 13, wherein

the external bus controller is adapted to receive a select signal from the arbiter for being controlled as a slave.

18. An article comprising: a storage medium, said storage medium having stored thereon instructions, that, when executed by at least one device, result in:

receiving a plurality of requests;

characterizing the received requests in terms of whether they would use one of a system bus of an on-chip system, an external bus of the system, and both the buses;

assigning priorities to the requests according to preset rankings;

selecting a first one of the requests having a top one of the priorities;

determining whether at least one of the system bus and the external bus that would be idle if the first request were granted; and

if so, selecting a second one of the requests that can be performed by at least one of the would-be idle buses, and then granting concurrently the first request and the second request.

19. The article of claim 18, wherein the instructions further result in:

determining whether a request having a second one of the priorities can be the second request.

20. The article of claim 18, wherein the instructions further result in:

if the request having the second one of the priorities can not be the second request, determining whether a request having a third one of the priorities can be the second request.

21. An article comprising: a storage medium, said storage medium having stored thereon instructions, that, when executed by at least one device, result in:

granting a request by an on-chip multi-jurisdictional multi-channel general direct memory access (mJmCGDMA) block to control only a system bus in an on-chip system; and

then granting a request by the mJmCGDMA block to control only an external bus in an off-chip system.

22. The article of claim 21, wherein the instructions further result in:

then granting a request by the mJmCGDMA block to control both the system bus and the external bus concurrently.

23. A method for a semiconductor chip having a plurality of on-chip functional blocks, at least one on-chip system bus for connecting at least some of the blocks, and an external bus for at least one of the functional blocks to exchange data with off-chip devices, the method comprising:

receiving a plurality of requests;

characterizing the received requests in terms of whether they would use one of the system bus, the external bus, and both the buses;

selecting a first one of the requests;

identifying the buses that would be idle if the first request were performed;

selecting a second one of the requests that can be performed by at least one of the system bus and the external bus that would be idle if the first request were performed; and

granting the second request concurrently with granting the first request.

24. The method of claim 23, further comprising:

assigning respective non-hierarchical priorities to all the requests by a single chip multi-jurisdictional arbiter,

wherein the first request is the one with a top one of the priorities.

25. The method of claim 23, further comprising:

identifying all buses on the chip that would be idle if the first request and the second request were performed concurrently;

selecting a third one of the requests that can be performed by an auxiliary system bus on the chip which would be idle if the first request and the second request were performed concurrently; and

granting the third request concurrently with granting the first request.

26. The method of claim 23, further comprising:

transferring a first set of data through the system bus pursuant to the granted first request;

transferring a second set of data through the external bus pursuant to the granted second request concurrently with transferring the first set of data; and

transferring a third set of data through the auxiliary system bus pursuant to the granted third request concurrently with transferring the first set of data.

27. The method of claim 23, further comprising:

transferring a single set of data through the auxiliary system bus, the system bus, and the external bus pursuant to the granted first, second and third requests.

28. A method for a semiconductor chip having an on-chip CPU block, a second on-chip functional block, at least one on-chip system bus for connecting the on-chip blocks, a on-chip DRAM refresh controller and an external bus, the method comprising:

receiving a plurality of requests, a first one of which being from the DRAM refresh controller;

examining whether a second one of the remaining requests is for using only the system bus; and

if so, granting the first and second requests to be performed concurrently.

29. The method of claim 28, further comprising:

assigning priorities to the requests;

selecting a request having a second one of the priorities; and

determining whether the selected request can be the second request.

30. The method of claim 28, further comprising:

if the request having the second one of the priorities can not be the second request, determining whether a request having a third one of the priorities can be the second request.

31. A method for a semiconductor chip having a plurality of on-chip functional blocks, at least one on-chip system bus for connecting at least some of the blocks, and an external bus for at least one of the functional blocks to exchange data with off-chip devices, the method comprising:

receiving a plurality of requests;

characterizing the received requests in terms of whether they would use one of the system bus, the external bus, and both the buses;

assigning priorities to the requests according to preset rankings;

selecting a first one of the requests having a top one of the priorities;

determining whether at least one of the system bus and the external bus that would be idle if the first request were granted; and

if so, selecting a second one of the requests that can be performed by at least one of the would-be idle buses, and then granting concurrently the first request and the second request.

32. The method of claim 31, further comprising:

determining whether a request having a second one of the priorities can be the second request.

33. The method of claim 32, further comprising:

if the request having the second one of the priorities can not be the second request, determining whether a request having a third one of the priorities can be the second request.

34. A method for a semiconductor chip having an on-chip multi-jurisdictional multi-channel general direct memory access (mJmCGDMA) block, a second on-chip functional block, at least one on-chip system bus for connecting the on-chip blocks, and an external bus for the mJmCGDMA block to exchange data with an off-chip device, the method comprising:

granting a request by the mJmCGDMA block to control only the system bus in a first cycle; and

then granting a request by the mJmCGDMA block to control the only external bus in a second cycle subsequent to the first cycle.

35. The method of claim 34, further comprising:

then granting a request by the mJmCGDMA block to control the system bus and the external bus concurrently in a third cycle subsequent to the second cycle.